

## CLAIMS

What is claimed is:

- 1     1.     A method for determining data stored by a memory cell having a  
2     select gate coupled to a wordline, a first electrode coupled to a bitline, and a  
3     second electrode coupled to a conductor, comprising the steps of:  
4         floating the bitline;  
5         applying a first voltage to the wordline;  
6         applying a second voltage to the conductor such that the bitline is  
7             set to a third voltage that is equal to the first voltage minus a  
8             threshold voltage of the memory cell; and  
9         sensing the third voltage to determine the data stored by the  
10         memory cell.
- 1     2.     The method of claim 1, further comprising an initial step of setting  
2     the bitline to a ground potential.
- 1     3.     The method of claim 1, wherein the memory cell is a nonvolatile  
2     memory cell.
- 1     4.     A method for simultaneously determining data stored by a plurality  
2     of memory cells each having a select gate coupled to a wordline, a first  
3     electrode coupled to one of a plurality of bitlines, and a second electrode  
4     coupled to a conductor, comprising the steps of:  
5         floating the plurality of bitlines;  
6         applying a first voltage to the wordline;  
7         applying a second voltage to the conductor such that the plurality of  
8             bitlines is set to a plurality of third voltages, wherein one of the  
9             plurality of third voltages is equal to the first voltage minus a  
10             threshold voltage of one of the plurality of memory cells; and

11           sensing the plurality of third voltages to determine the data stored  
12           by the plurality of memory cells.

1     5.     The method of claim 4, further comprising an initial step of setting  
2     the plurality of bitlines to a ground potential.

1     6.     The method of claim 4, wherein the plurality of memory cells are  
2     nonvolatile memory cells.

1     7.     The method of claim 4, wherein determining the data stored by the  
2     plurality of memory cells comprises reading a page of data.

1     8.     A method for determining data stored by a memory cell having an  
2     adjustable threshold voltage, a select gate coupled to a wordline, a first  
3     electrode coupled to a bitline, and a second electrode coupled to a  
4     conductor, comprising the steps of:  
5         floating the bitline;  
6         applying a first voltage to the wordline;  
7         applying a second voltage to the conductor such that the bitline is  
8         set to a third voltage;  
9         determining the adjustable threshold voltage of the memory cell  
10        based on the third voltage; and  
11        determining the data stored in the memory cell based on the  
12        adjustable threshold voltage of the memory cell.

1     9.     A memory device comprising:  
2     a memory array having data stored in a memory cell, the memory  
3     cell having a select gate coupled to a wordline, a first electrode  
4     coupled to a bitline, and a second electrode coupled to a  
5     conductor; and

6 a periphery circuit coupled to the memory array, the periphery  
7 circuit transmitting a first voltage to the wordline and  
8 transmitting a second voltage to the conductor such that the  
9 bitline is set to a third voltage that is equal to the first voltage  
10 minus a threshold voltage of the memory cell, wherein the  
11 periphery circuit senses the third voltage to determine the data  
12 stored by the memory cell.

1 10. The memory device of claim 9, wherein the periphery circuit  
2 further transmits a ground potential to the bitline before transmitting the  
3 first voltage or the second voltage to the memory cell.

1 11. The memory device of claim 9, wherein the memory cell is a  
2 nonvolatile memory cell.

1 12. The memory device of claim 9, wherein the periphery circuit  
2 comprises:  
3 a voltage regulation circuit outputting the first voltage and the  
4 second voltage;  
5 a voltage switching circuit coupling the second voltage to the  
6 memory cell; and  
7 a sensing circuit coupled to the memory cell, wherein the sensing  
8 circuit senses the third voltage to determine the data stored by  
9 the memory cell.

1 13. The memory device of claim 12, further comprising:  
2 a decoder circuit receiving the first voltage from the voltage  
3 switching circuit and coupling the first voltage to the memory  
4 cell, the decoder circuit decoding a location of the memory cell in  
5 the memory array.

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1 14. The memory device of claim 12, further comprising:  
2 a control circuit having read circuitry and write circuitry each  
3 coupled to the voltage regulation circuit, the voltage switching  
4 circuit, and the ~~sense~~<sup>sensing</sup> circuit, wherein the control circuit controls  
5 when the first voltage and the second voltage are supplied to the  
6 memory cell and when the third voltage is sensed by the ~~sense~~<sup>sensing</sup>  
7 circuit.

1 15. The memory device of claim 12, wherein the sensing circuit  
2 comprises:  
3 an analog-to-digital converter circuit operative to receive the third  
4 voltage and generate a digital value.

1 16. A memory device comprising:  
2 a memory array having data stored in a plurality of memory cells,  
3 the plurality of memory cells each having a select gate coupled to  
4 a wordline, a first electrode coupled to one of a plurality of  
5 bitlines, and a second electrode coupled to a conductor; and  
6 a periphery circuit coupled to the memory array, the periphery  
7 circuit transmitting a first voltage to the wordline and  
8 transmitting a second voltage to the conductor such that the  
9 plurality of bitlines is set to a plurality of third voltages, wherein  
10 one of the plurality of third voltages is equal to the first voltage  
11 minus a threshold voltage of one of the plurality of memory  
12 cells, and wherein the periphery circuit simultaneously senses  
13 the plurality of third voltages to determine the data stored by the  
14 memory array.

1 17. A memory device comprising:  
2 a memory array having data stored in a memory cell having an  
3 adjustable threshold voltage; and  
4 a periphery circuit coupled to the memory array, the periphery  
5 circuit transmitting a plurality of voltages to the memory cell  
6 and sensing the adjustable threshold voltage of the memory cell  
7 to determine the data stored by the memory cell.

o 1 18. A memory device comprising:  
2 means having an adjustable threshold <sup>voltage string</sup> for ~~strong~~ data; and  
3 means coupled to the storing means for determining the data stored  
4 in the storing means by sensing the adjustable threshold voltage.